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Birch Stewart Kolash & Birch LLP
Post Office Box 747
Falls Church, VA 22040-0747

EXAMINER	
HERNANDEZ, NELSON D	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/635,847	KONISHI ET AL.	
	Examiner	Art Unit	
	Nelson D. Hernandez	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18,21,29-31 and 33-44* is/are rejected.

7)☒ Claim(s) *19,20,22-28 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/27/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The Examiner acknowledges the amendments made to the Specifications. The amendments made are accepted.

Response to Amendment

2. The Examiner acknowledges the amended claims filed on January 8, 2007. Claims 4, 11, 12, 15, 18 and 32 have been amended. Claims 33-44 have been newly added.

Response to Arguments

3. Applicant's arguments with respect to claims 1, 7, 9, 10, 14 and 15 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

4. **Claim 12** is objected to because of the following informalities: in lines 2-4, the limitation "directly processes the stored first image signal produce the corresponding second image signal" should read "directly processes the stored first image signal to produce the corresponding second image signal". Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

6. **Claims 7, 8, 10, 25, 27, 29, 30, 31, 34, 36, 38, 39, 41 and 43** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. **Claim 7** recites the limitation "a plurality of image processors for each performing image processing, different from each other, on the stored first image signal to produce **a third image signal different from each other**;" in page 10, lines 1-3. The limitation as written requires a single image signal to be different from each other rendering the limitation as indefinite for failing to pointing out and distinctly claim the subject matter, and also rendering the limitation "a second memory for storing therein **the third image signals produced**" (see page 10, line 4) to have insufficient antecedent basis. Is the limitation meant to read "a plurality of image processors for each performing image processing, different from each other, on the stored first image signal to produce a plurality of third image signals different from each other"?

8. **Claims 8, 25, 29, 30, 34, 38 and 41** are also rejected under 35 U.S.C. 112, second paragraph, as being dependent from **claim 7**.

9. **Claim 10** recites the limitation "a plurality of image processors for each performing image processing, different from each other, on the stored first image signal to produce **the second image signal different from each other**" in lines 5-7. There is insufficient antecedent basis for this limitation in the claim. Also, the limitation requires

a single image signal to be different from each other, rendering the limitation as indefinite for failing to pointing out and distinctly claim the subject matter and further rendering the limitation "a second memory for storing therein **the second image signals produced**" (see line 8) to have insufficient antecedent basis. Is the limitation meant to read "a plurality of image processors for each performing image processing, different from each other, on the stored first image signal to produce ~~the~~ a plurality of second image signals different from each other"?

10. **Claims 27, 31, 36, 39 and 43** are also rejected under 35 U.S.C. 112, second paragraph, as being dependent from **claim 10**.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 9, 12, 14-16 and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Kawamura et al., US Patent 5,821,997.

Regarding claim 9, Kawamura et al. discloses a method of processing a first image signal (to be stored in memory 1 as shown in fig. 5) representative of an image of a subject field captured by an imaging device (electronic camera; col. 1, lines 19-21) to produce a plurality of second image signals (to be stored in memory card 4 as shown in fig. 5), comprising the steps of: storing the first image signal in a first memory (first

image signal is stored in memory 1 as shown in fig. 5); performing image processing on the stored first image signal according to parameters of image processing different from each other to produce the plurality of second image signals (the first image signal is processed to generate a plurality of images compressed with different compression ratios; col. 2, line 38 – col. 3, line 17 (this teaches that the parameters between the image processing made are different)); and storing each of the produced plurality of second image signals in a second memory (the produced images with different compression ration are stored in memory card 4 as shown in fig. 5), wherein the second memory is a non-volatile memory (memory card 4 is not a volatile memory) (Col. 2, line 38 – col. 4, line 42).

Regarding claim 12, Kawamura et al. discloses that the each of said plurality of image processing directly processes the stored first image signal to produce the corresponding second image signal (See Kawamura, the processor 2 receives the image signal directly from the memory 1).

Regarding claim 14, Kawamura discloses an image processing method, comprising: retrieving a first image data (to be stored in memory 1 as shown in fig. 5); generating a plurality of second image data (to be stored in memory card 4 as shown in fig. 5) based (using image processor 2 as shown in fig. 5) on the first image data; and storing each of the plurality of second image data into a memory (Fig. 5: 4), wherein a combination of imaging parameters and values applied to generate each second image data is unique for each second image data among the plurality of second image data (the first image signal is processed to generate a plurality of images compressed with

different compression ratios; col. 2, line 38 – col. 3, line 17 (this teaches that the parameters between the image processing made are different (each combination of imaging parameters and values applied to generate each second image data is unique for each second image data among the plurality of second image data))), and wherein the memory is a non-volatile memory (memory card 4 is not a volatile memory) (Col. 2, line 38 – col. 4, line 42).

Regarding claim 15, Kawamura et al. discloses that the step of generating the plurality of second image data includes directly processing the first image data when generating each of the plurality of second image data (the processor 2 receives the image signal directly from the memory 1 as shown in fig. 5).

Regarding claim 16, claim 16 is written in a Markush type by using the expression "include at least one of gain, gradation control, luminance-chrominance, edge enhancement, saturation emphasis, and compression ratio", meeting one species of a genus family anticipates the claimed subject matter. "A generic claim cannot be allowed to an applicant if the prior art discloses a species falling within the claimed genus." The species in that case will anticipate the genus. In re Slayter, 276 F.2d 408, 411, 125 USPQ 345, 347 (CCPA 1960); In re Gosteli, 872 F.2d 1008, 10 USPQ2d 1614 (Fed. Cir. 1989).

Kawamura et al. discloses that the imaging parameters include compression ratio (Col. 2, line 38 – col. 3, line 17).

Regarding claim 35, Kawamura et al. discloses that the first (memory 1 as shown in fig. 5) and second memories (memory card 4 as shown in fig. 5) are different from each other (See fig. 5).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 1, 2, 6, 11, 33, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawamura et al., US Patent 5,821,997 in view of Ishihara, US Patent 6,091,513.

Regarding claim 1, Kawamura et al. discloses an image signal processor (See fig. 5) for performing image processing on a first image signal (to be stored in memory 1 as shown in fig. 5) representative of an image of a subject field captured by an imaging device (electronic camera; col. 1, lines 19-21) to produce a plurality of second image signals (to be stored in memory card 4 as shown in fig. 5), comprising: a first memory (Fig. 5: 1) for storing the first image signal; an image processor (Fig. 5: 2) for performing a plurality of different image processing (different compression ratios; col. 2, line 38 – col. 3, line 17) on the stored first image signal to produce the plurality of second image signals (plurality of images obtained by compressing the first image signal with different compression ratios), wherein all second image signals are different from each other

different compression ratios; col. 2, line 38 – col. 3, line 17); and a second memory (memory card 4 as shown in fig. 5) for storing each of the plurality of second image signals produced, wherein said plurality of image processors include types and parameters (compression ratios) of the image processing such that at least one of the types and parameters of the image processing are different between said plurality of image processing processors (the image is processed to generate a plurality of images compressed with different compression ratios; col. 2, line 38 – col. 3, line 17 (this teaches that the parameters between the processing made by the image processor are different)), and wherein said second memory is a non-volatile memory (memory card 4 is not a volatile memory) (Col. 2, line 38 – col. 4, line 42).

Although Kawamura et al. teaches performing a plurality of image processing to the image signal, Kawamura et al. teaches performing said plurality of image processing with a single image processor and not with a plurality of image processors as claimed.

However, the concept of performing a plurality of image processing each having parameters different form each other with multiple image processor is notoriously well known in the art as taught by Ishihara. Ishihara teaches an image signal processor (Fig. 6: 18) for performing image processing on a first image signal (original image 36 as shown in fig. 6) representative of an image of a subject field to produce a plurality of second image signals (See images in memory 30 as shown in fig. 6), comprising: a memory (Fig. 6: 34; Ishihara also discloses that the image signal processor may also comprise a main memory for loading the processing program) for storing the first image signal; a plurality of image processors (Fig. 6, items 24, 26, 28, 30 and 32) for each

performing image processing on the stored first image signal to produce the plurality of second image signals, wherein all second image signals are different from each other (See images different from each other in memory 30 as shown in fig. 6); and a memory (Memory 34 as shown in fig. 34) for storing each of the plurality of second image signals produced, wherein said plurality of image processors include types and parameters of the image processing such that at least one of the types and parameters of the image processing are different between said plurality of image processors (The image is being recorded at different resolutions, this reads as having different parameters) (Col. 18, line 65 – col. 19, line 10) (Col. 12, line 4 – col. 13, line 48).

Therefore, taking the combined teaching of Kawamura et al. in view of Ishihara as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kawamura et al. by performing said plurality of image processing with a plurality of image processors. The motivation to do so would have been to have a dedicated image processor for each image processing performed to the image signal thus the processing would be performed faster as opposed to when using a single image processor.

Regarding claim 2, claim 2 is written in a Markush type by using the expression "include at least one selected from a group consisting of a change of brightness, a change of gradation change characteristics, a correction of a color temperature, a change of saturation, a change of a contour, a change of a compression ratio and a change of a black level of the first image signal stored in said first memory", meeting one species of a genus family anticipates the claimed subject matter. "A generic claim

cannot be allowed to an applicant if the prior art discloses a species falling within the claimed genus." The species in that case will anticipate the genus. In re Slayter, 276 F.2d 408, 411, 125 USPQ 345, 347 (CCPA 1960); In re Gosteli, 872 F.2d 1008, 10 USPQ2d 1614 (Fed. Cir. 1989).

The combined teaching of Kawamura et al. in view of Ishihara as discussed and analyzed in claim 1 teaches that the types of processing performed by each of said plurality of image processors (Ishihara, fig. 6, items 24, 26, 28, 30 and 32) include a change of a compression ratio (See Kawamura et al., col. 2, line 38 – col. 3, line 17). Grounds for rejecting claim 1 apply here.

Regarding claim 6, Kawamura et al discloses that the second memory (Fig. 5: 4) is detachably connected to said image signal processor (Kawamura et al. inherently discloses that the second memory is a detachably connected by teaching the use of a card interface 3 for communicating with the memory card 3. Card interfaces are notoriously well known in the art as used to connect removable memory cards to communicate with the camera).

Regarding claim 11, the combined teaching of Kawamura et al. in view of Ishihara as discussed and analyzed in claim 1 teaches that each of said plurality of image processors is configured to directly process the stored first image signal to produce the corresponding second image signal (See Kawamura, the processor 2 receives the image signal directly from the memory 1; see also See Ishihara, col. 12, line 4 – col. 13, line 48). Grounds for rejecting claim 1 apply here.

Regarding claim 33, Kawamura et al. discloses that the first (memory 1 as shown in fig. 5) and second memories (memory card 4 as shown in fig. 5) are different from each other (See fig. 5).

Regarding claim 37, Kawamura et al. discloses that the first (memory 1 as shown in fig. 5) and second memories (memory card 4 as shown in fig. 5) are different from each other (See fig. 5).

15. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawamura et al., US Patent 5,821,997 in view of Ishihara, US Patent 6,091,513 and further in view of Boies, US Patent 5,426,732.

Regarding claim 3, the combined teaching of Kawamura et al. in view of Ishihara fails to teach that each of said plurality of image processors corresponds to one of a plurality of display units which are provided for visualizing the images represented by the plurality of second image signals stored in said second memory, each of said plurality of image processors processing, according to the parameters, the plurality of second image signals to be displayed on one of the plurality of display units which corresponds to said image processor.

However, Boies discloses an image signal processor (See figs. 1: 26 and 3: 26) for performing image processing on a first image signal representative of an image of a subject field captured by an imaging device to produce a plurality of second image signals, comprising: a first memory (Fig. 1: 24) for storing the first image signal; a plurality of image processors (See fig. 3, processors 42, 44 and 46 in the display

processing unit 26) for each performing image processing on the stored first image signal to produce the plurality of second signals, wherein all second image signals are different fro each other (see images in display screen 30 shown in figs. 1 and 2, displaying the images with different image transformation done (image pan, tilt, and zoom transformations)); and a second memory (Fig. 1: 28) for storing each of the plurality of second image signals produced, wherein said plurality of image processors include types and parameters of the image processing are different between said plurality of image processors (image pan, tilt, and zoom transformations) (Col. 4, lines 21-55; col. 6, line 42 – col. 7, line 6). Boies also discloses that the generated images can be sent to a printer to obtain a hard copy of said generated images (Col. 5, lines 22-32) and that each of said plurality of image processors (fig. 3, processors 42, 44 and 46 in the display processing unit 26) corresponds to a plurality of display units (figs. 1: 30 and 2: 30) unit which are provided for visualizing the images represented by the plurality of second image signals (See fig. 1 and 2) stored in said second memory (See fig. 1: 28), each of said plurality of image processors processing, according to the parameters, the plurality of second image signals to be displayed on one of the plurality of display units which corresponds to said image processor. (Col. 4, lines 21-55; col. 6, line 42 – col. 7, line 6).

Therefore, taking the combined teaching of Kawamura et al. in view of Ishihara and further in view of Boies as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kawamura et al. and Ishihara by having each of said plurality of image processors corresponding to one of a

plurality of display units which are provided for visualizing the images represented by the plurality of second image signals stored in said second memory, each of said plurality of image processors processing, according to the parameters, the plurality of second image signals to be displayed on one of the plurality of display units which corresponds to said image processor. The motivation to do so would have been to provide a process control system user interface that derives one or more next states of a system based upon a current state of the system and upon a computational model of the system, and which furthermore provides a visual display of the one or more derived next states in conjunction with a visual display of the current state as suggested by Boies (col. 2, lines 3-18).

Regarding claim 4, the combined teaching of Kawamura et al. in view of Ishihara and further in view of Boies as discussed and analyzed in claim 1 teaches that the plurality of display units include a display (See Ishihara, Col. 19, lines 11-17; Boies teaches using a display screen in fig. 1: 30) and an image printer (See Ishihara, col. 9, line 31 – col. 10, line 44; Boies, col. 5, lines 22-32).

16. Claims 5, 7, 8, 10, 13, 29-31, 34, 36, 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawamura et al., US Patent 5,821,997 in view of Ishihara, US Patent 6,091,513 and further in view of Moriya, US Patent 5,754,709.

Regarding claim 5, the combined teaching of Kawamura et al. in view of Ishihara fails to teach a divider circuit for dividing the first image signal stored in said first memory into a highlight area and a shadow area, each of said plurality of image

processors performing the image processing in which at least one of the types and the parameters of the image processing differs between the highlight area and the shadow area.

However, Moriya teaches a method an apparatus for gradation correction and image edge extraction (See figs. 4(a) and 4(b)), comprising an image dividing means for dividing the image into dark and bright areas in order to perform gradation correction to de divided image, wherein the dark image is subjected to gradation correction (See fig. 4(b): 4) while the bright image is left as it is (this teaches that the second images as processed using different parameters). After the images are processed separately, they are synthesized by an image synthesizing means (Fig. 4(b): 5) and output by the image output means (Fig. 4(b): 7) (Col. 2, lines 35-65; col. 5, lines 16-50; col. 6, lines 6-25).

Therefore, taking the combined teaching of Kawamura et al. in view of Ishihara and further in view of Moriya as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kawamura et al. and Ishihara by having the image processors performing a change of gradation change characteristics to the first image signal stored in said first memory by having each of said plurality of image processors performing the image processing in which at least one of the types and the parameters of the image processing differs between the highlight area and the shadow area. The motivation to do so would have been to accurately extract the edges of a region within an image as suggested by Moriya (Col. 2, lines 43-48).

Regarding claim 7, Kawamura et al. discloses an image signal processor (Fig. 5) for performing image processing on a first image signal (to be stored in memory 1 as shown in fig. 5) representative of an image of a subject field captured by an imaging device to produce a second image signal (to be stored in memory card 4 as shown in fig. 5), comprising: a first memory (Fig. 5: 1) for storing therein the first image signal; an image processor (Fig. 5: 2) performing a plurality of image processing, different from each other (different compression ratios; col. 2, line 38 – col. 3, line 17), on the stored first image signal to produce a third image signal (plurality of images compressed at different compression ratio) different from each other (to be stored in memory card 4 as shown in fig. 5); a second memory (Fig. 5: 4) for storing therein the third image signals produced; and wherein said plurality of image processors include types and parameters (compression ratios) of the image processing such that at least one of the types and parameters of the image processing are different between said plurality of image processing processors (the image is processed to generate a plurality of images compressed with different compression ratios; col. 2, line 38 – col. 3, line 17 (this teaches that the parameters between the processing made by the image processor are different)), and wherein said second memory is a non-volatile memory (memory card 4 is not a volatile memory) (Col. 2, line 38 – col. 4, line 42) ((Kawamura et al. also discloses that the user may select from among the plurality third image signal (which is a plurality of compressed images generated from the first image signal (image stored in memory 1)) in order to stored the most adequate compressed image in the memory card so that the other compressed images are deleted; col. 3, lines 7-67)).

Kawamura et al. teaches performing a plurality of image processing to the image signal, Kawamura et al. teaches performing said plurality of image processing with a single image processor and not with a plurality of image processors as claimed and having an image composer circuit for composing the third image signals to produce the second image signal.

However, the concept of performing a plurality of image processing each having parameters different form each other with multiple image processor is notoriously well known in the art as taught by Ishihara. Ishihara teaches an image signal processor (Fig. 6: 18) for performing image processing on a first image signal (original image 36 as shown in fig. 6) representative of an image of a subject field to produce a plurality of second image signals (See images in memory 30 as shown in fig. 6), comprising: a memory (Fig. 6: 34; Ishihara also discloses that the image signal processor may also comprise a main memory for loading the processing program) for storing the first image signal; a plurality of image processors (Fig. 6, items 24, 26, 28, 30 and 32) for each performing image processing on the stored first image signal to produce the plurality of second image signals, wherein all second image signals are different from each other (See images different from each other in memory 30 as shown in fig. 6); and a memory (Memory 34 as shown in fig. 34) for storing each of the plurality of second image signals produced, wherein said plurality of image processors include types and parameters of the image processing such that at least one of the types and parameters of the image processing are different between said plurality of image processors (The image is being

recorded at different resolutions, this reads as having different parameters) (Col. 18, line 65 – col. 19, line 10) (Col. 12, line 4 – col. 13, line 48).

Therefore, taking the combined teaching of Kawamura et al. in view of Ishihara as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kawamura et al. by performing said plurality of image processing with a plurality of image processors. The motivation to do so would have been to have a dedicated image processor for each image processing performed to the image signal thus the processing would be performed faster as opposed to when using a single image processor.

The combined teaching of Kawamura et al. in view of Ishihara fails to teach having an image composer circuit for composing the third image signals to produce the second image signal.

However, Moriya teaches a method an apparatus for gradation correction and image edge extraction (See figs. 4(a) and 4(b)), comprising an image dividing means for dividing the image (the Examiner is reading this as a first image signal) into dark and bright areas (the Examiner is reading the dark and bright areas as a plurality of third image signals generated from the first image signal) in order to perform gradation correction to de divided image, wherein the dark image is subjected to gradation correction (See fig. 4(b): 4) while the bright image is left as it is (this teaches that the plurality of third image signals are processed using different parameters). After the images are processed separately (processing the plurality of third image signals independently), they are synthesized by an image synthesizing means (Fig. 4(b): 5) and

output by the image output means (Fig. 4(b): 7) (this teaches the creation of the second image signal by composing a plurality of third image signals) (Col. 2, lines 35-65; col. 5, lines 16-50; col. 6, lines 6-25).

Therefore, taking the combined teaching of Kawamura et al. in view of Ishihara and further in view of Moriya as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kawamura et al. and Ishihara by having the image processors performing a change of gradation change characteristics to the first image signal stored in said first memory by having each of said plurality of image processors performing the image processing in which at least one of the types and the parameters of the image processing differs between the highlight area and the shadow area and to have an image composer circuit for composing the plurality of third image signals to produce the second image signal. The motivation to do so would have been to accurately extract the edges of a region within an image and to improve the dynamic range of the image signal by composing the plurality of processed third image signals as suggested by Moriya (Col. 1, line 63 – col. 2, line 48).

Regarding claim 8, limitations can be found in claim 7.

Regarding claim 10, claim 10 is written in a Markush type by using the expression "include at least one selected from a group consisting of a change of brightness, a change of gradation change characteristics, a correction of a color temperature, a change of saturation, a change of a contour, a change of a compression ratio and a change of a black level of the first image signal stored in said first memory",

meeting one species of a genus family anticipates the claimed subject matter. "A generic claim cannot be allowed to an applicant if the prior art discloses a species falling within the claimed genus." The species in that case will anticipate the genus. In re Slayter, 276 F.2d 408, 411, 125 USPQ 345, 347 (CCPA 1960); In re Gosteli, 872 F.2d 1008, 10 USPQ2d 1614 (Fed. Cir. 1989).

Kawamura et al discloses an imaging apparatus (Fig. 5) comprising: an imaging device (electronic camera; col. 1, lines 19-21) for capturing an image of a subject field and producing a first image signal (to be stored in memory 1 as shown in fig. 5) representative of the subject field; a first memory (Fig. 5: 4) for storing therein the first image signal; an image processor (Fig. 5: 2) performing a plurality of image processing, different from each other (different compression ratios; col. 2, line 38 – col. 3, line 17), on the stored first image signal to produce the second image signal (a plurality of compressed images at different compression ratio) different from each other; and a second memory (memory card 4 as shown in fig. 5) for storing therein the second image signals produced; said plurality of image processors include types and parameters (compression ratios) of the image processing such that at least one of the types and parameters of the image processing are different between said plurality of image processing processors (the image is processed to generate a plurality of images compressed with different compression ratios; col. 2, line 38 – col. 3, line 17 (this teaches that the parameters between the processing made by the image processor are different)); the types of image processing including a change of a compression ratio (col. 2, line 38 – col. 3, line 17) of the first image signal stored in said first memory,

whereby said image processor perform the plurality of image processing according to the parameters (different compression ratios) of image processing to the first image signal stored in said first memory (Col. 2, line 38 – col. 4, line 42) ((Kawamura et al. also discloses that the user may select from among the plurality third image signal (which is a plurality of compressed images generated from the first image signal (image stored in memory 1)) in order to stored the most adequate compressed image in the memory card so that the other compressed images are deleted; col. 3, lines 7-67)).

Kawamura et al. teaches performing a plurality of image processing to the image signal, Kawamura et al. teaches performing said plurality of image processing with a single image processor and not with a plurality of image processors as claimed and having an image composer circuit for composing the second image signals to produce a third image signal.

However, the concept of performing a plurality of image processing each having parameters different form each other with multiple image processor is notoriously well known in the art as taught by Ishihara. Ishihara teaches an image signal processor (Fig. 6: 18) for performing image processing on a first image signal (original image 36 as shown in fig. 6) representative of an image of a subject field to produce a plurality of second image signals (See images in memory 30 as shown in fig. 6), comprising: a memory (Fig. 6: 34; Ishihara also discloses that the image signal processor may also comprise a main memory for loading the processing program) for storing the first image signal; a plurality of image processors (Fig. 6, items 24, 26, 28, 30 and 32) for each performing image processing on the stored first image signal to produce the plurality of

second image signals, wherein all second image signals are different from each other (See images different from each other in memory 30 as shown in fig. 6); and a memory (Memory 34 as shown in fig. 34) for storing each of the plurality of second image signals produced, wherein said plurality of image processors include types and parameters of the image processing such that at least one of the types and parameters of the image processing are different between said plurality of image processors (The image is being recorded at different resolutions, this reads as having different parameters) (Col. 18, line 65 – col. 19, line 10) (Col. 12, line 4 – col. 13, line 48).

Therefore, taking the combined teaching of Kawamura et al. in view of Ishihara as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kawamura et al. by performing said plurality of image processing with a plurality of image processors. The motivation to do so would have been to have a dedicated image processor for each image processing performed to the image signal thus the processing would be performed faster as opposed to when using a single image processor.

The combined teaching of Kawamura et al. in view of Ishihara fails to teach having an image composer circuit for composing the second image signals to produce a third image signal.

However, Moriya teaches a method an apparatus for gradation correction and image edge extraction (See figs. 4(a) and 4(b)), comprising an image dividing means for dividing the image (the Examiner is reading this as a first image signal) into dark and bright areas (the Examiner is reading the dark and bright areas as a plurality of second

image signals generated from the first image signal) in order to perform gradation correction to de divided image, wherein the dark image is subjected to gradation correction (See fig. 4(b): 4) while the bright image is left as it is (this teaches that the plurality of second image signals are processed using different parameters). After the images are processed separately (processing the plurality of second image signals independently), they are synthesized by an image synthesizing means (Fig. 4(b): 5) and output by the image output means (Fig. 4(b): 7) (this teaches the creation of the third image signal by composing a plurality of second image signals) (Col. 2, lines 35-65; col. 5, lines 16-50; col. 6, lines 6-25).

Therefore, taking the combined teaching of Kawamura et al. in view of Ishihara and further in view of Moriya as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kawamura et al. and Ishihara by having the image processors performing a change of gradation change characteristics to the first image signal stored in said first memory by having each of said plurality of image processors performing the image processing in which at least one of the types and the parameters of the image processing differs between the highlight area and the shadow area and to have an image composer circuit for composing the plurality of second image signals to produce the third image signal. The motivation to do so would have been to accurately extract the edges of a region within an image and to improve the dynamic range of the image signal by composing the plurality of processed third image signals as suggested by Moriya (Col. 1, line 63 – col. 2, line 48).

Regarding claim 13, limitations can be found in claim 5.

Regarding claim 29, Kawamura et al. discloses that the second memory is non-volatile ((memory card 4 is not a volatile memory) (Col. 2, line 38 – col. 4, line 42).

Regarding claim 30, Kawamura et al. discloses that the second memory is non-volatile ((memory card 4 is not a volatile memory) (Col. 2, line 38 – col. 4, line 42).

Regarding claim 31, Kawamura et al. discloses that the second memory is non-volatile ((memory card 4 is not a volatile memory) (Col. 2, line 38 – col. 4, line 42).

Regarding claim 34, Kawamura et al. discloses that the first (memory 1 as shown in fig. 5) and second memories (memory card 4 as shown in fig. 5) are different from each other (See fig. 5).

Regarding claim 36, Kawamura et al. discloses that the first (memory 1 as shown in fig. 5) and second memories (memory card 4 as shown in fig. 5) are different from each other (See fig. 5).

Regarding claim 38, the combined teaching of Kawamura et al. in view of Ishihara and further in view of Moriya as discussed and analyzed in claim 7, teaches that each of the plurality of image processors is configured to directly process the stored first image signal to produce the corresponding third image signal (See Kawamura, the processor 2 receives the image signal directly from the memory 1). Grounds for rejecting claim 7 apply here.

Regarding claim 39, the combined teaching of Kawamura et al. in view of Ishihara and further in view of Moriya as discussed and analyzed in claim 10, teaches that each of the plurality of image processors is configured to directly process the stored

first image signal to produce the corresponding third image signal (See Kawamura, the processor 2 receives the image signal directly from the memory 1). Grounds for rejecting claim 10 apply here.

17. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawamura et al., US Patent 5,821,997 in view of Boies, US Patent 5,426,732.

Regarding claim 17, Kawamura et al. does not explicitly disclose that the step of generating the plurality of second image data includes particularizing at least one second image data for a display type.

However, Boies discloses an image signal processor (See figs. 1: 26 and 3: 26) for performing image processing on a first image signal representative of an image of a subject field captured by an imaging device to produce a plurality of second image signals, comprising: a first memory (Fig. 1: 24) for storing the first image signal; a plurality of image processors (See fig. 3, processors 42, 44 and 46 in the display processing unit 26) for each performing image processing on the stored first image signal to produce the plurality of second signals, wherein all second image signals are different fro each other (see images in display screen 30 shown in figs. 1 and 2, displaying the images with different image transformation done (image pan, tilt, and zoom transformations)); and a second memory (Fig. 1: 28) for storing each of the plurality of second image signals produced, wherein said plurality of image processors include types and parameters of the image processing are different between said plurality of image processors (image pan, tilt, and zoom transformations) (Col. 4, lines

21-55; col. 6, line 42 – col. 7, line 6). Boies also discloses that the generated images can be sent to a printer to obtain a hard copy of said generated images (Col. 5, lines 22-32) and that each of said plurality of image processors (fig. 3, processors 42, 44 and 46 in the display processing unit 26) corresponds to a plurality of display units (figs. 1: 30 and 2: 30) unit which are provided for visualizing the images represented by the plurality of second image signals (See fig. 1 and 2) stored in said second memory (See fig. 1: 28), each of said plurality of image processors processing, according to the parameters, the plurality of second image signals to be displayed on one of the plurality of display units which corresponds to said image processor. (Col. 4, lines 21-55; col. 6, line 42 – col. 7, line 6).

Therefore, taking the combined teaching of Kawamura et al. in view of Boies as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kawamura et al. by generating the plurality of second image data includes particularizing at least one second image data for a display type. The motivation to do so would have been to provide a process control system user interface that derives one or more next states of a system based upon a current state of the system and upon a computational model of the system, and which furthermore provides a visual display of the one or more derived next states in conjunction with a visual display of the current state as suggested by Boies (col. 2, lines 3-18).

Regarding claim 18, the combined teaching of Kawamura et al. in view of Boies as discussed and analyzed in claim 17 teaches that the display type is one of a display

(Boies teaches using a display screen in fig. 1: 30) or a printer (Boies, col. 5, lines 22-32).

18. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawamura et al., US Patent 5,821,997 in view of Moriya, US Patent 5,754,709.

Regarding claim 21, Kawamura et al. does not explicitly disclose dividing the first image data into a plurality of areas, each area differing in brightness; adjusting the brightness of the plurality of areas by a corresponding plurality of adjustment amounts; and combining the adjusted plurality of areas.

However, Moriya teaches a method an apparatus for gradation correction and image edge extraction (See figs. 4(a) and 4(b)), comprising an image dividing means for dividing the image into dark and bright areas in order to perform gradation correction to de divided image, wherein the dark image is subjected to gradation correction (See fig. 4(b): 4) while the bright image is left as it is (this teaches that the second images as processed using different parameters). After the images are processed separately, they are synthesized by an image synthesizing means (Fig. 4(b): 5) and output by the image output means (Fig. 4(b): 7) (Col. 2, lines 35-65; col. 5, lines 16-50; col. 6, lines 6-25).

Therefore, taking the combined teaching of Kawamura et al. in view of Moriya as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kawamura et al. by dividing the first image data into a plurality of areas, each area differing in brightness; adjusting the brightness of the plurality of areas by a corresponding plurality of adjustment amounts; and combining the

adjusted plurality of areas. The motivation to do so would have been to accurately extract the edges of a region within an image as suggested by Moriya (Col. 2, lines 43-48).

19. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawamura et al., US Patent 5,821,997 in view of Ishihara, US Patent 6,091,513 and further in view of Kotaki, US Patent 5,337,152.

Regarding claim 40, the combined teaching of Kawamura et al. in view of Ishihara teaches that at least one of the plurality of image processors is configured to independently perform image processing the stored first image signal to produce the corresponding second image signal but fails to teach that at least one of the plurality of image processors is configured to independently perform image processing on each color of the image signal.

However, having a plurality of processors wherein each of the processors is configured to independently perform image processing on each color signal of an image is notoriously well known in the art as taught by Kotaki. Kotaki teaches a camera (Fig. 2) comprising a plurality of image processors (See fig. 2, processors 40, 39 and 38) configured to independently perform image processing on each color (Red, Green and Blue) of the image signal to produce a plurality of second image signals for further processing said plurality of second image signals (Col. 4, line 30 – col. 5, line 31).

Therefore, taking the combined teaching of Kawamura et al. in view of Ishihara and further in view of Kotaki as a whole, it would have been obvious to one of ordinary

skill in the art at the time the invention was made to modify Kawamura et al. and Ishihara by having at least one of the plurality of image processors is configured to independently perform image processing on each color of the image signal. The motivation to do so would have been to have a dedicated image processor for each color in to the image signal thus the color processing would be performed faster as opposed to when using a single image processor to perform complicated image processing (i.e. color demosaicing, zoom, etc.) that would reduce the speed of the image processor.

20. Claims 41 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawamura et al., US Patent 5,821,997 and Ishihara, US Patent 6,091,513 in view of Moriya, US Patent 5,754,709 and further in view of Kotaki, US Patent 5,337,152.

Regarding claim 41, the combined teaching of Kawamura et al. in view of Ishihara and further in view of Moriya teaches independently performing, for at least one set of parameters of image processing, image processing the stored first image signal to produce the corresponding plurality of third image signals but fails to teach independently performing, for at least one set of parameters of image processing, image processing on each color.

However, having a plurality of processors wherein each of the processors is configured to independently perform image processing on each color signal of an image is notoriously well known in the art as taught by Kotaki. Kotaki teaches a camera (Fig.

2) comprising a plurality of image processors (See fig. 2, processors 40, 39 and 38) configured to independently perform image processing on each color (Red, Green and Blue) of the image signal to produce a plurality of second image signals for further processing said plurality of second image signals (Col. 4, line 30 – col. 5, line 31).

Therefore, taking the combined teaching of Kawamura et al. and Ishihara in view of Moriya and further in view of Kotaki as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kawamura et al., Ishihara and Moriya by having at least one of the plurality of image processors is configured to independently perform image processing on each color of the image signal. The motivation to do so would have been to have a dedicated image processor for each color in to the image signal thus the color processing would be performed faster as opposed to when using a single image processor to perform complicated image processing (i.e. color demosaicing, zoom, etc.) that would reduce the speed of the image processor.

Regarding claim 43, limitations scan be found in claim 41.

21. Claims 42 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawamura et al., US Patent 5,821,997 in view of Ishihara, US Patent 6,091,513 and further in view of Kotaki, US Patent 5,337,152.

Regarding claim 42, Kawamura et al. discloses independently performing, for at least one set of parameters of image processing, image processing the stored first image signal to produce the corresponding second image signal but does not explicitly

disclose independently performing, for at least one set of parameters of image processing, image processing on each color.

However, having a plurality of processors wherein each of the processors is configured to independently perform image processing on each color signal of an image is notoriously well known in the art as taught by Kotaki. Kotaki teaches a camera (Fig. 2) comprising a plurality of image processors (See fig. 2, processors 40, 39 and 38) configured to independently perform image processing on each color (Red, Green and Blue) of the image signal to produce a plurality of second image signals for further processing said plurality of second image signals (Col. 4, line 30 – col. 5, line 31).

Therefore, taking the combined teaching of Kawamura et al. in view of Ishihara and further in view of Kotaki as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kawamura et al. and Ishihara by having at least one of the plurality of image processors is configured to independently perform image processing on each color of the image signal. The motivation to do so would have been to have a dedicated image processor for each color in to the image signal thus the color processing would be performed faster as opposed to when using a single image processor to perform complicated image processing (i.e. color demosaicing, zoom, etc.) that would reduce the speed of the image processor.

Regarding claim 44, limitations can be found in claim 42.

Allowable Subject Matter

22. **Claims 19, 20, 22-28 and 32** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

23. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 19, the main reason for indication of allowable subject matter is because the prior art fails to teach or reasonably suggest determining whether a brightness of the first predetermined maximum or below a predetermined minimum; and performing a black level correction on the first image data if the brightness of the first image data is determined to be above the predetermined image data is above a maximum or below the predetermined minimum in combination with all the limitations in claim 14.

Regarding claim 22, the main reason for indication of allowable subject matter is because the prior art fails to teach or reasonably suggest that the step of adjusting the brightness includes reducing the brightness of the highlight area and increasing the brightness of the shadow area including all the existing limitations of claims 14 and 21.

Regarding claim 24, the main reason for indication of allowable subject matter is because the prior art fails to teach or reasonably suggest a data compressor configured to compress the plurality of second image signals prior to being stored in the second memory, wherein a compression ratio for compressing each of the plurality of second

image signals is based on a type of the display unit designated for the second image in combination with all the limitations in claims 1 and 3.

Regarding claim 25, the main reason for indication of allowable subject matter is because the prior art fails to teach or reasonably suggest a data compressor configured to compress the second image signal, wherein a compression ratio for compressing the second image signal is based on a type of the display unit designated for the second image signal in combination with all the limitations in claim 7.

Regarding claim 26, the main reason for indication of allowable subject matter is because the prior art fails to teach or reasonably suggest determining a compression ratio for each of the plurality of second image signals based on a type of the display unit designated for the second image signal, and compressing each of the plurality of second image signals prior storing in the second memory with the determined compression ratio in combination with all the limitations in claim 9.

Regarding claim 27, the main reason for indication of allowable subject matter is because the prior art fails to teach or reasonably suggest a data compressor configured to compress the third image signal, wherein a compression ratio for compressing the third image signal is based on a type of the display unit designated for the third image signal in combination with all the limitations in claim 10.

Regarding claim 28, the main reason for indication of allowable subject matter is because the prior art fails to teach or reasonably suggest determining a compression ratio for each of the plurality of second image data based on a type of the display unit designated for the second image data, and compressing each of the plurality of second

image data prior storing in the second memory with the determined compression ratio in combination with all the limitations in claim 14.

Conclusion

24. Because a new ground for rejection is being applied to unamended independent claims 1, 7, 9, 10 and 14, this action will be **Non-Final**.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson D. Hernandez whose telephone number is (571) 272-7311. The examiner can normally be reached on 8:30 A.M. to 6:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivek Srivastava can be reached on (571) 272-7304. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Nelson D. Hernandez
Examiner
Art Unit 2622

NDHH
April 28, 2007

VIVEK SRIVASTAVA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600